IN THE CLAIMS

Please amend the claims as follows:

1-20. (Cancelled)

21. (Currently Amended) A differential output structure, comprising:

an input line including:

a first path having an input end for receiving an input signal, the first path also having an output end and including at least one driving element, and

a second path having an input end and operably coupled to the input end of the first path for receiving the input signal, the second path also having an output end;

an output driver, operably coupled to the output ends of the first and second paths, that is configured to provide differential outputs; and

a bi-directional sync circuit, operably coupled between the first and second paths, which is configured to synchronize the speed of signals traveling on the two paths to arrive at the output driver by dynamically synchronizing the two paths bi-directionally through the sync circuit; the bi-directional sync circuit having a single connection to the first path and a single connection to the second path and being sized in accordance with relative connection positions in the first and second paths.

22. (Previously Presented) The structure of claim 21,

wherein the first path further includes a plurality of driving elements connected in series to one another, the first path providing an inverted output of the input signal and

wherein the second path includes a plurality of driving elements connected in series to one another, the second path providing a non-inverted output of the input signal.

23. (Previously Presented) The structure of claim 22, wherein the driving elements of the first and second paths have a predetermined constant taper ratio.

24. (Currently Amended) The structure of claim 22, wherein each sync circuit is coupled between an output of a driving element on the first path having a first current driving capability and an output of a driving element on the second path having a second current driving capability, and-- wherein the first current driving capability is greater than the second current driving capability.

25. (Previously Presented) The structure of claim 21, further includes at least another sync circuit, operably coupled between the first and second paths, that is configured to synchronize the speed of signals traveling on the two paths.

26. (Currently Amended) The structure of claim 25, wherein each of the sync circuits includes a capacitance.

27. (Previously Presented) The structure of claim 21, wherein the sync circuit includes a capacitance.

28. (Previously Presented) The structure of claim 21, wherein the sync circuit is coupled

between the output ends of the first and second paths.

29. (Previously Presented) The structure of claim 21, wherein the sync circuit dynamically synchronizes the two paths by slowing down a faster of the two paths such that the signals of the two paths arrive at the output driver at substantially a same time.

30. (Currently Amended) A differential output structure, comprising:

an input line including:

a first path having an input end for receiving an input signal, the first path also having an output end and including at least one driving element, and

a second path having an input end and operably coupled to the input end of the first path for receiving the input signal, the second path also having an output end and including at least one driving element;

an output driver, operably coupled to the output ends of the first and second paths, that is configured to provide differential outputs; and

a plurality of bi-directional sync circuits, operably coupled between the first and second paths, which ~~is~~ are configured to synchronize the speed of signals traveling on the two paths to arrive at the output driver by bidirectionally synchronizing the two paths through the synch circuits;

the bi-directional sync circuits each having a single connection to the first path and a single connection to the second path, the sync circuits being sized relative to their position along each of the first and second paths and the connections being disposed between respective driving elements.

31. (Previously Presented) The structure of claim 30,

wherein the first path further includes a plurality of driving elements connected in series to one another, the first path providing an inverted output of the input signal and

wherein the second path includes a plurality of driving elements connected in series to one another, the second path providing a non-inverted output of the input signal.

32. (Previously Presented) The structure of claim 31, wherein the driving elements of the first and second paths have a predetermined constant taper ratio.

33. (Previously Presented) The structure of claim 31, wherein each sync circuit is coupled between an output of a driving element on the first path having a first current driving capability and an output of a driving element on the second path having a second current driving capability, and wherein the first current driving capability is greater than the second current driving capability.

34. (Previously Presented) The structure of claim 30, further includes at least another sync circuit, operably coupled between the first and second paths, that is configured to synchronize the speed of signals traveling on the two paths.

35. (Previously Presented) The structure of claim 34, wherein each of the sync circuits includes a capacitance

36. (Previously Presented) The structure of claim 30, wherein the sync circuit includes a capacitance.

37. (Previously Presented) The structure of claim 30, wherein the sync circuit is coupled between the output ends of the first and second paths.

38. (Previously Presented) The structure of claim 30, wherein the sync circuit bidirectionally synchronizes the two paths by slowing down a faster of the two paths such that the signals of the two paths arrive at the output driver at substantially a same time.

39. (Currently Amended) A differential output structure, comprising:

an input line including:

a first path having an input and including at least one driving element, and

a second path operably coupled to the first path at the input end for receiving an input signal;

an output driver, operably coupled to output ends of the first and second paths; and

a bi-directional sync circuit, operably coupled between the first and second paths, which is configured to synchronize the speed of signals traveling on the two paths to arrive at the output driver by bidirectionally synchronizing the two paths through the synch circuit to slow a faster of the two paths, the bi-directional sync circuit having a single connection to the first path and a single connection to the second path and being sized in accordance with relative connection positions

in the first and second paths.

40. (Previously Presented) The structure of claim 39, wherein the faster of the two paths is slowed such that the signals of the two paths arrive at the output driver at substantially a same time.